Claims

[c1] 1.A virtual full-crossbar logic emulator comprising:

a plurality of logic chips with programmable logic gates for programming to emulate a target design for emulation;

logic pins on each of the logic chips, the logic pins for connecting signals in the target design connecting to programmable logic gates in different logic chips;

a row of column routing chips with programmable interconnection, the column routing chips having routing pins coupled to the logic pins of the logic chips; and

a sub-row of diagonal routing chips with programmable interconnection, the diagonal routing chips having routing pins coupled to a subset of the logic pins of the logic chips;

wherein the logic pins of the logic chips include a first group of the logic pins, each logic pin in the first group coupled to a single column routing chip; and a second group of the logic pins, each logic pin in the second group coupled to a column routing chip and coupled to a diagonal routing chip;

whereby connections between logic chips are programmably made by the column routing chips and by the diagonal routing chips.

[c2] 2.The virtual full-crossbar logic emulator of claim 1 wherein routing pins of column routing chips connected to logic pins in the second group that are also connected to a diagonal routing chip and are being used by a diagonal routing chip for an active connection are disabled in the column routing chip,

whereby routing pins are disabled in the column routing chip when a connected logic pin is used for a connection by a diagonal logic chip.

[c3] 3.The virtual full-crossbar logic emulator of claim 2 wherein routing pins of diagonal routing chips connected to logic pins that are being used by a column routing chip for an active connection are disabled in the diagonal routing chip,

whereby routing pins are disabled in the diagonal routing chip when a connected logic pin is used for a connection by a column logic chip.

[c4] 4.The virtual full-crossbar logic emulator of claim 3 wherein each logic chip in the plurality of logic chips comprises a first set of the logic pins, a second set of the logic pins, a third set of the logic pins, and a fourth set of the logic pins;

wherein each column routing chip in the row of column routing chips connects to only one of the sets of the logic pins, each column routing chip connecting to a same set of the logic pins of each of the logic chips and not connecting to other sets of the logic pins; and

wherein each routing chip in the sub-row of diagonal routing chips connects to a different set of the logic pins for different logic chips,

whereby column routing chips connect to a same set of the logic pins while diagonal routing chips connect to different sets of the logic pins.

[c5] 5.The virtual full-crossbar logic emulator of claim 4 wherein the logic pins are divided into P sets of the logic pins, wherein P is a number of column routing chips, the P sets including the first set, the second set, the third set, and the fourth set;

wherein each column routing chip connects to the logic chips through a different set of the P sets of logic pins.

[c6] 6.The virtual full-crossbar logic emulator of claim 5 wherein each column routing chip connects to all logic chips.

[c7] 7.The virtual full-crossbar logic emulator of claim 5 wherein connections between the logic chips are represented by a routing table having rows and columns, each row in the routing table representing a logic chip, each column in the routing table representing a set of the logic pins;

wherein each of the column routing chips is for making connections within a single column in the routing table;

wherein each of the diagonal routing chips is for making connections spanning several columns of the routing table.

[c8] 8.The virtual full-crossbar logic emulator of claim 7 wherein connections made by diagonal routing chips fall along diagonal lines in the routing table, each diagonal line spanning at least two columns and two rows of the routing table.

[c9] 9.The virtual full-crossbar logic emulator of claim 8 wherein each diagonal routing chip is coupled to all logic chips;
wherein each diagonal routing chip is coupled to all sets of the logic pins,
whereby the diagonal routing chips fall on diagonal lines that span all columns in the routing table.

[c10] 10.The virtual full-crossbar logic emulator of claim 8 wherein each diagonal routing chip is coupled to all logic chips;
wherein each diagonal routing chip is coupled to less than all sets of the logic pins,
whereby the diagonal routing chips fall on diagonal lines that span fewer than all columns in the routing table, the diagonal routing chips being within a region of the routing table.

[c11] 11.The virtual full-crossbar logic emulator of claim 5 wherein the sub-row of the diagonal routing chips comprises fewer routing chips than contained in the row of column routing chips.

[c12] 12.The virtual full-crossbar logic emulator of claim 11 wherein the sub-row of the diagonal routing chips contains one-half of a number of routing chips in the row of column routing chips,
whereby the sub-row is a half-row.

[c13] 13.The virtual full-crossbar logic emulator of claim 12 wherein the row of column routing chips contains a same number of chips as the plurality of logic chips while the sub-row of diagonal routing chips contains one-half of a number of chips in the plurality of logic chips.

[c14] 14.The virtual full-crossbar logic emulator of claim 13 wherein each logic chip comprises a first number of logic pins, and wherein each routing chip

also comprises the first number of logic pins.

[c15] 15.The virtual full-crossbar logic emulator of claim 14 wherein the routing pins of the column routing chips are coupled to all logic pins including the second group of the logic pins;
wherein each logic pin in the second group of the logic pins is coupled both to a routing pin of a column routing chip and to a routing pin of a diagonal routing chip.

[c16] 16.The virtual full-crossbar logic emulator of claim 5 wherein the logic chips and the routing chips are field-programmable gate arrays (FPGA) chips.

[c17] 17.The virtual full-crossbar logic emulator of claim 16 wherein the logic chips and the routing chips are re-programmable.

[c18] 18.A logic emulator comprising:
first logic chip means for emulating logic gates of a target design for emulation, the first logic chip means having first, second, third, and fourth pin means for externally connecting logic gates;
second logic chip means for emulating logic gates of a target design for emulation, the second logic chip means having first, second, third, and fourth pin means for externally connecting logic gates;
third logic chip means for emulating logic gates of a target design for emulation, the third logic chip means having first, second, third, and fourth pin means for externally connecting logic gates;
fourth logic chip means for emulating logic gates of a target design for emulation, the fourth logic chip means having first, second, third, and fourth pin means for externally connecting logic gates;
first column routing chip means, having pin means for coupling to the first pin means of the first, second, third, and fourth logic chip means, for forming programmable connections among the first pin means of the first, second, third, and fourth logic chip means;
second column routing chip means, having pin means for coupling to the second pin means of the first, second, third, and fourth logic chip means, for

forming programmable connections among the second pin means of the first, second, third, and fourth logic chip means;

third column routing chip means, having pin means for coupling to the third pin means of the first, second, third, and fourth logic chip means, for forming programmable connections among the third pin means of the first, second, third, and fourth logic chip means;

fourth column routing chip means, having pin means for coupling to the fourth pin means of the first, second, third, and fourth logic chip means, for forming programmable connections among the fourth pin means of the first, second, third, and fourth logic chip means;

first column routing chip means, having pin means for coupling to the first pin means of the first, second, third, and fourth logic chip means, for forming programmable connections among the first pin means of the first, second, third, and fourth logic chip means;

first diagonal routing chip means, having pin means for coupling to the first pin means of the first logic chip means, to the second pin means of the second logic chip means, to the third pin means of the third logic chip means, and to the fourth pin means of the fourth logic chip means, for forming programmable connections among the first, second, third, and fourth pin means of the first, second, third, and fourth logic chip means; and

second diagonal routing chip means, having pin means for coupling to the fourth pin means of the first logic chip means, to the third pin means of the second logic chip means, to the second pin means of the third logic chip means, and to the first pin means of the fourth logic chip means, for forming programmable connections among the fourth, third, second, and first pin means of the first, second, third, and fourth logic chip means,

whereby emulated logic gates of the first, second, third, and fourth logic chip means are programmably connected by column and diagonal routing chips means.

[c19] 19.The logic emulator of claim 18 wherein the first, second, third, and fourth pin means comprise one or more signal pins.

[c20] 20.A virtual full-crossbar emulator comprising:

a plurality of L field-programmable gate array (FPGA) logic chips, each logic chip for emulating logic gates and each logic chip having signal pins for externally connecting to other logic chips;

wherein the signal pins comprise P pin sets;

a plurality of P column routing chips, each column routing chip coupled to the L FPGA logic chips using a same one of the P pin sets, each column routing chip for making programmable connections between FPGA logic chips using one of the P pin sets; and

a plurality of P/2 diagonal routing chips, each diagonal routing chip coupled to the L FPGA logic chips using different ones of the P pin sets, each diagonal routing chip for making programmable connections between FPGA logic chips using different ones of the P pin sets;

wherein L and P are integers greater than one,

whereby the programmable connections are made within a pin set using a column routing chip, but made between pin sets using a diagonal routing chip.